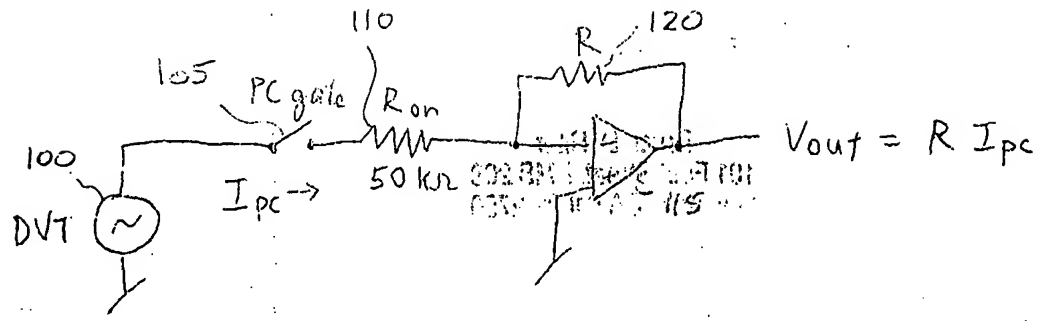
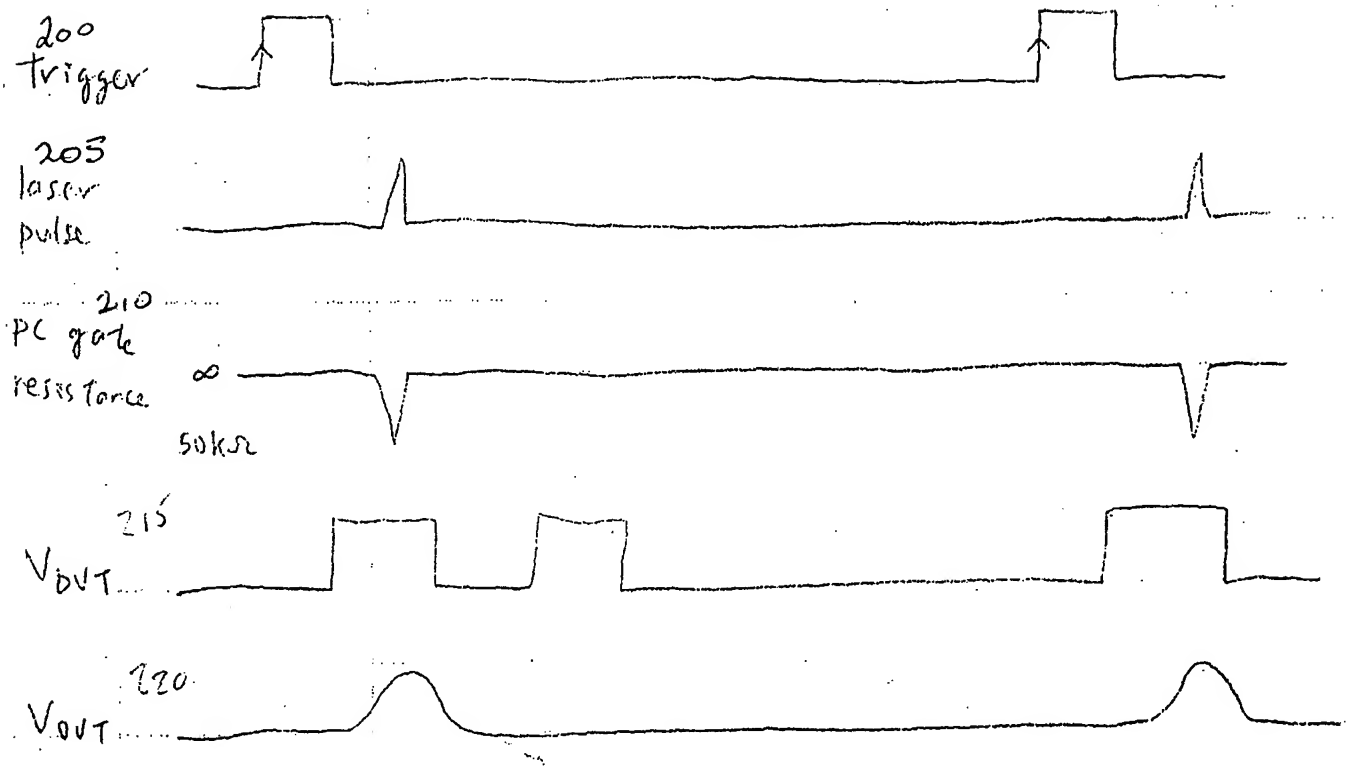
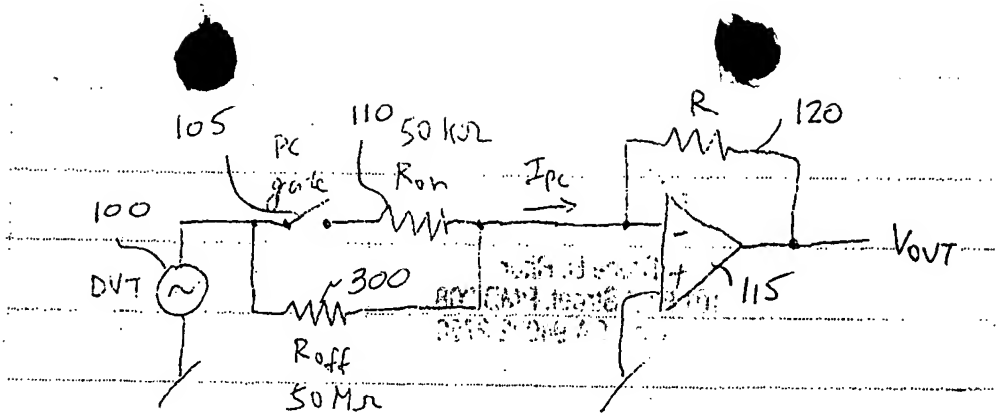


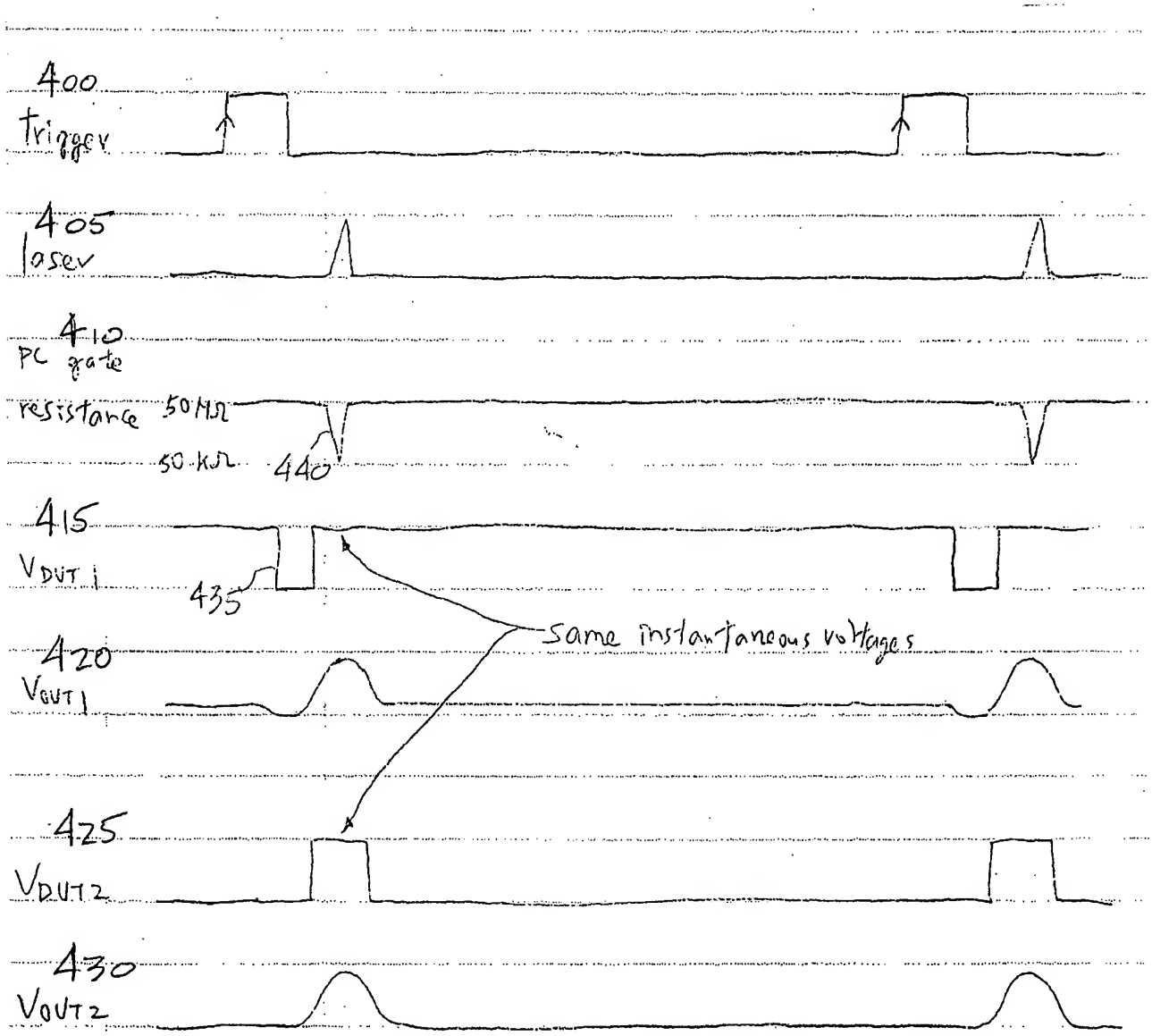
Prior Art
Figure 1



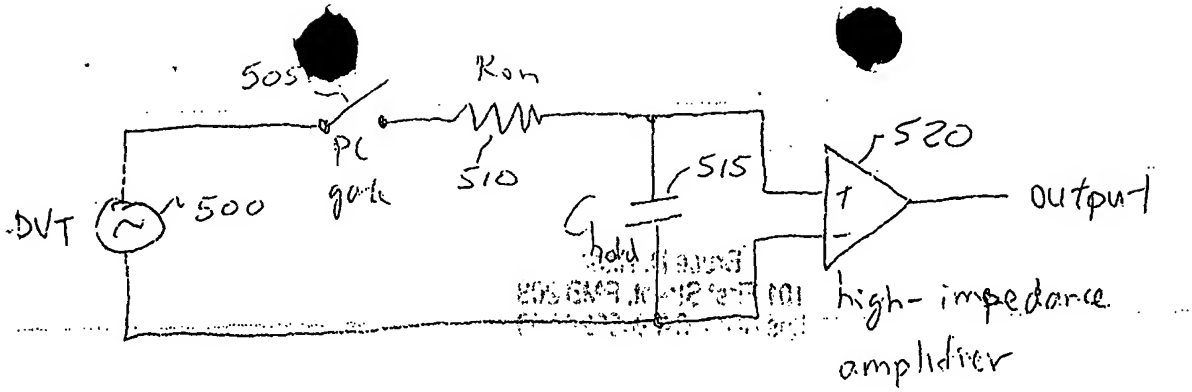
Prior Art
Figure 2



Prior Art
Figure 3



Prior Art
Figure 4



Prior Art
Figure 5

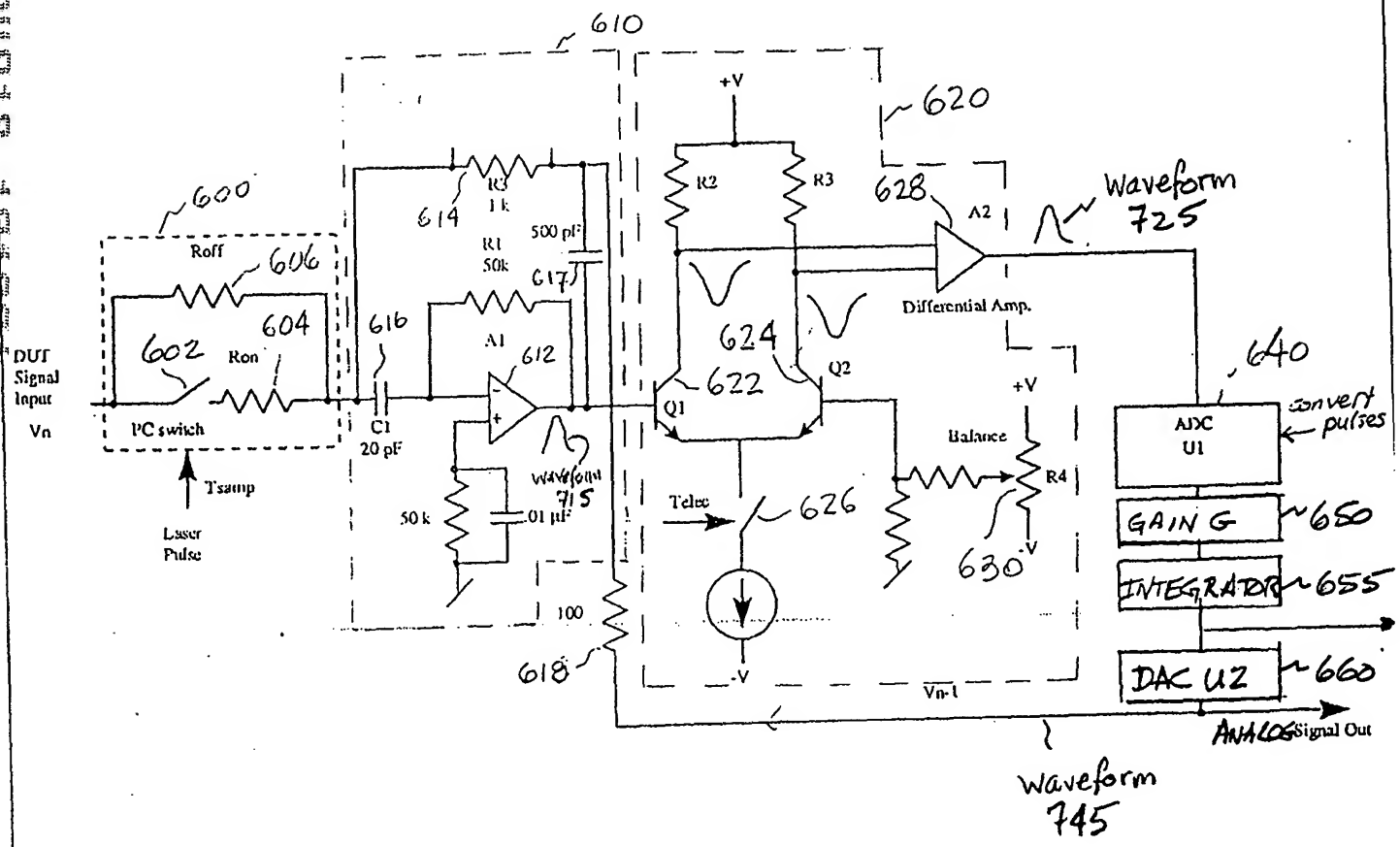


Figure 6

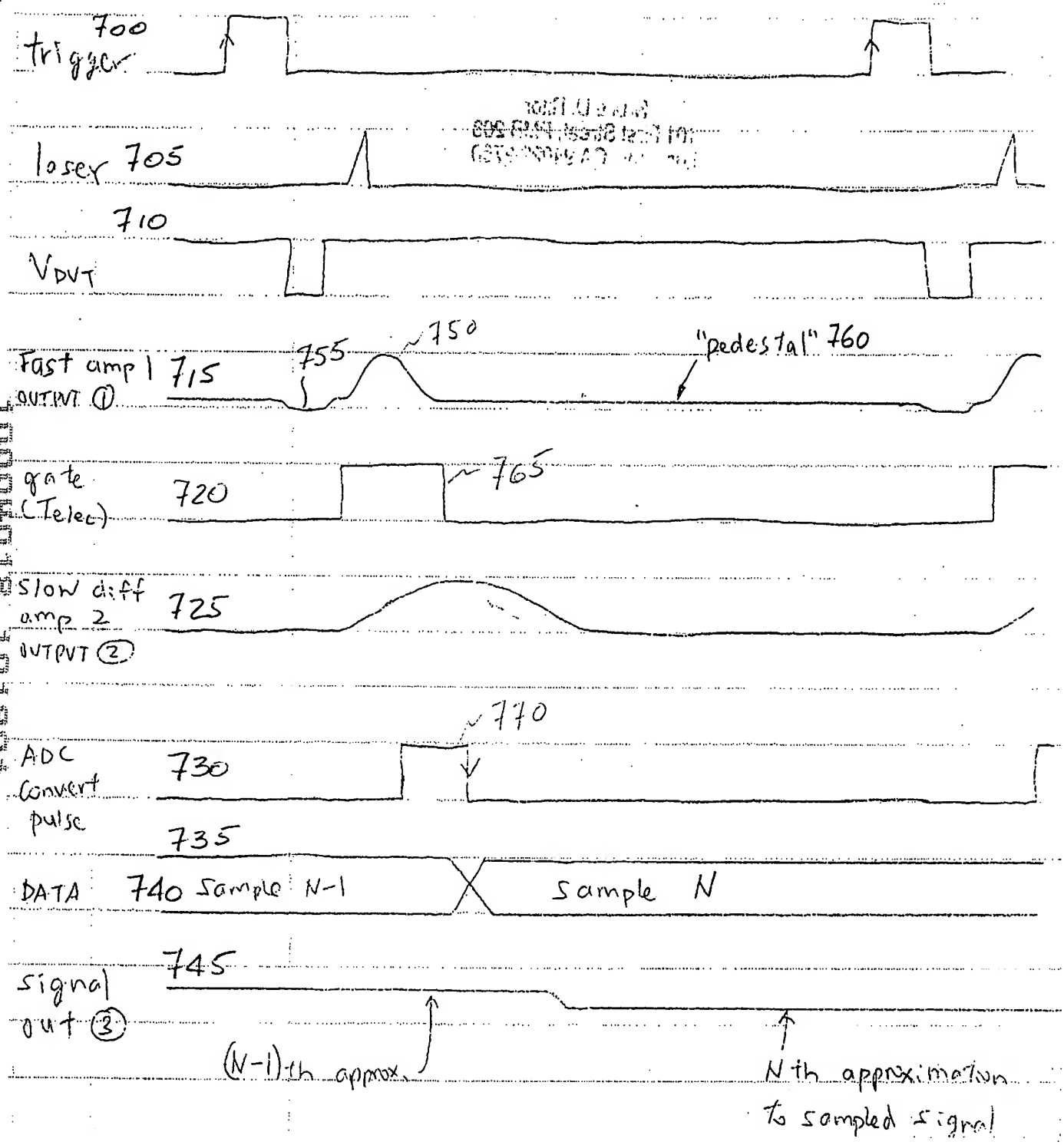

700
trigger
laser 705
710
VDUT
Fast amp 1 715
OUTPUT ①
755
750
"pedestal" 760
gate (Telec) 720
765
slow diff amp 2
OUTPUT ②
725
770
ADC convert pulse
730
735
DATA 740
Sample N-1
Sample N
745
signal out ③
(N-1)th approx.
Nth approximation to sampled signal

Figure 7

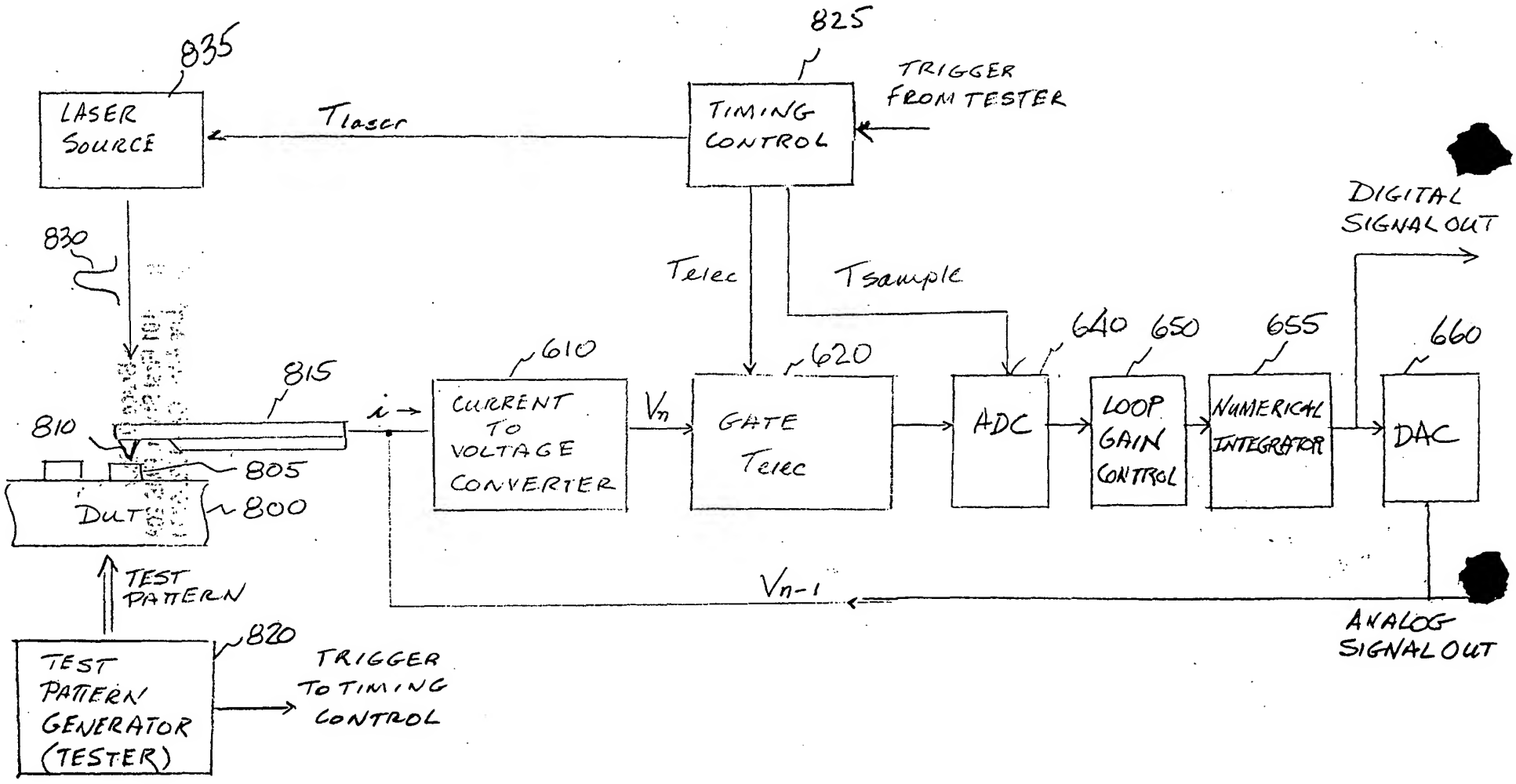

835
LASER SOURCE
Tlaser
825
TIMING CONTROL
TRIGGER FROM TESTER
DIGITAL SIGNAL OUT
830
Telec
Tsample
640
650
655
660
815
610
620
810
805
800
CURRENT TO VOLTAGE CONVERTER
Vn
GATE Telec
ADC
LOOP GAIN CONTROL
NUMERICAL INTEGRATOR
DAC
DUT
TEST PATTERN
Vn-1
ANALOG SIGNAL OUT
820
TEST PATTERN GENERATOR (TESTER)
TRIGGER TO TIMING CONTROL

Figure 8